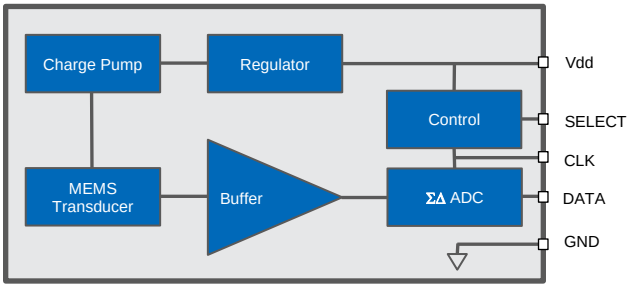
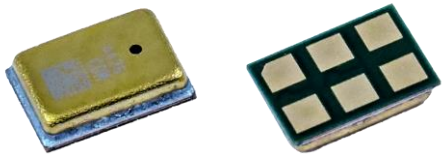
V2S200DZ
MULTIMODE DIGITAL VIBRATION SENSOR

The V2S200DZ is a miniature, high-performance, low power, digital Voice Vibration Sensor (V2S) with a single bit PDM output. Derived from Syntiant's proven high performance SiSonic™ MEMS technology, the V2S200D consists of a transducer, a low-noise input buffer, and a sigma-delta modulator. These devices provide high vibration sensitivity suitable for picking up audio via bone conduction in devices such as earphones, wearables, and other applications where flat response to vibration and excellent acoustic isolation are required. In addition, the V2S200D offers multiple clock modes for wide compatibility with audio codecs.





PRODUCT FEATURES

- Low Current Consumption in Low-Power Mode
- Wide Sensor Bandwidth (10 kHz)
- High Drive Capability
- Supports Dual Multiplexed Channels
- Multiple Performance Modes (Sleep,Low-Power,Normal)
- Ultra-Stable Performance
- IPX7 Rating
- Standard SMD Reflow
- LGA Package

TYPICAL APPLICATIONS

- Earphones
- Wind Noise Reduction
- Self Speech Detection
- Imposter Rejection
- Wearables, Smart Watches
- Medical Applications, Sethoscopes

ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Ratings

Parameter	Absolute Maximum Rating	Units
Vdd to Ground	-0.5, +5.0	V
DATA, CLOCK, SELECT to Ground	-0.3, +5.0	V
Input Current	±5	mA
Short Circuit to/from DATA	Indefinite to Ground or Vdd	sec
Storage Temperature	-40 to +100	ºC
Operating Temperature	-40 to +85	ºC

Stresses exceeding these "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation at these or any other conditions beyond those indicated under "Performance & Electrical Specifications" is not implied. Exposure beyond those indicated under "Performance & Electrical Specifications" for extended periods may affect device reliability.

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PERFORMANCE & ELECTRICAL SPECIFICATIONS[1]

Table 2: General Sensor Specifications
Test Conditions: 23 ±2° C, 55 ±20% R.H., Vdd = 1.8 V, Tedge ≤ 3 ns, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	Vdd		1.65	1.8	3.3	V
Bandwidth	BW		-	10	-	kHz
High Frequency Flatness		+3dB relative to 1 kHz	-	4	-	kHz
Resonant Frequency Peak	Fres	Acceleration response	-	7	-	kHz
Sound Isolation[2]		Output ratio, 1g peak input vs 94dB input @ 100 Hz	-	>70	-	dB
		Output ratio, 1g peak input vs 94dB input @ 1 kHz	-	>70	-	
DC Offset		Fullscale = ±100 (SEL = Low / SEL = High)	-	0.0/0.78	-	%
Polarity		+ Z axis (Refer to Mechanical Specs for axis definition)	Increasing density of 1's			
Data Format			½ Cycle PDM			
Sensitivity Drop		Vdd(min) ≤ Vdd ≤ Vdd(max)	-	-	.5dB	dB
Clock Input Capacitance	Cin		-	5	-	pF
Data Output Load	Cload		-	-	160	pF
SELECT (high)			Vdd-0.2	-	3.3	V
SELECT (low)			-0.3	-	0.2	V
Short Circuit Current	Isc	Grounded DATA pin	1	-	20	mA
Startup Time[3]		Powered Down → Active, S within 1 dB of final value	-	-	20	ms
Time to First Data Bit[4]		Time from valid Vdd and CLK until the first logical bit is driven on the DATA line. The output is tristate until First Data Bit. Initial output bits represent muted audio. Audio data will follow Startup Time.	-	4	-	ms
Mode-Change Time[3, 4]		Low Power Mode ⇔ Normal Mode, S within 1 dB of final value	-	-	20	ms

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Table 3: Normal Mode
Test Conditions: 23 ±2° C, 55 ±20% R.H., Vdd = 1.8 V, Fclock = 2.4 MHz (D.C. = 50%), Tedge ≤ 3 ns, SELECT grounded, no load, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current[5]	Idd	Fclock = 1.2 MHz Fclock = 1.536 MHz Fclock = 2.4 MHz Fclock = 3.072 MHz	- - - -	480 550 700 850	- - - -	µA
Sensitivity	S	1g peak @ 1 kHz (Z-Axis)	-26	-25	-24	dBFS
G range		10% THD	-	±25	-	g peak
Signal to Noise Ratio	SNR	Sensitivity @ 1kHz, A-weighted (BW = 100 – 4 kHz) Fclock = 1.2 MHz Sensitivity @ 1kHz, A-weighted (BW = 100 – 4 kHz) Fclock = 1.536 MHz Sensitivity @ 1kHz, A-weighted (BW = 100 – 4 kHz) Fclock = 2.4 MHz Sensitivity @ 1kHz, A-weighted (BW = 100 – 4 kHz) Fclock = 3.072 MHz	- - - -	63.5 63.5 64.5 64.5	- - - -	dB(A)
Noise Density		@ 1 kHz	-	9	-	$\mu g/\sqrt{Hz}$
Total Harmonic Distortion	THD	1 g peak @ 1 kHz	-	.25	-	%
		1% THD @ 1 kHz, S = typ	-	>10	-	g peak
Power Supply Rejection Ratio	PSRR	200 mVpp sinewave @ 1 kHz	-	75	-	dB V/FS
Power Supply Rejection	PSR + N	200 mVpp 7/8 duty cycle rectangular waveform @ 217 Hz, A-weighted	-	-80	-	dBFS(A)

Table 4: Low-Power Mode
Test Conditions: 23 ±2° C, 55 ±20% R.H., Vdd = 1.8 V, Fclock = 768 kHz (D.C. = 50%), Tedge ≤ 3 ns, SELECT grounded, no load, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply current[5]	Idd		120	139	160	µA
Sensitivity	S	1g peak @ 1 kHz (Z-Axis)	-26.5	-25.5	-24.5	dBFS
G range		10% THD	-	±26	-	g peak
Signal to Noise Ratio	SNR	Sensitivity @ 1 kHz, A-weighted (BW = 100 – 4 kHz)	-	63	-	dB(A)
Noise Density		@ 1 kHz	-	11	-	$\mu g/\sqrt{Hz}$
Total Harmonic Distortion	THD	1g peak @ 1 kHz	-	.25	-	%
		1% THD @ 1 kHz, S = typ	-	>10	-	g peak
Power Supply Rejection Ratio	PSRR	200 mVpp sinewave @ 1 kHz	-	72	-	dB V/FS
Power Supply Rejection	PSR + N	200 mVpp 7/8 duty cycle rectangular waveform @ 217 Hz, A-weighted	-	-80	-	dBFS(A)

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Table 5: «Mode3»
Test Conditions: 23 ±2° C, 55 ±20% R.H., Vdd = 1.8 V, Fclock grounded, SELECT grounded, no load, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sleep Current	Isleep	CLOCK = Pulled Low, DATA = High-Z	-	.5	10	µA

[1] Sensitivity and Supply Current are 100% tested.

[2] Isolation measurements are setup limited at 70db. Sensor isolation is beyond what the setup can measure.

[3] Valid sensor states are: Powered Down Mode (mic off), Sleep Mode (low current, DATA = high-Z, fast startup), Low-Power Mode (low clock speed) and Normal Mode.

[4] Output is temporarily muted during the transition between any sensor state.

[5] Power consumption varies with Cload according to: ΔP = 1/3*DVdd*DVdd*ΔCload*Fclock.

Table 6: Digital Interface
Test Conditions: 23 ±2° C, 55 ±20% R.H., Vdd = 1.8 V, Tedge ≤ 3ns, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High[7]	Vih		0.7xVdd	-	3.3	V
Logic Input Low[7]	Vil		-0.3	-	.3xVdd	V
Logic Output High[7]	Voh	I_{OUT} = 2 mA	Vdd-0.45	-	Vdd	V
Logic Output Low[7]	Vol	I_{OUT} = 2 mA	0	-	0.45	V
Low→High Threshold[8]	Vl-h		-	-	0.7xVdd	V
High→Low Threshold[8]	Vh-l		0.3xVdd	-	-	V
Hysteresis Width[8]	Vhyst		0.10xVdd	-	0.29xVdd	V
Clock Frequency[7]	Fclock	Sleep Mode	-	-	0	kHz
		Low-Power Mode	600	-	950	
		Normal Mode	1.2	-	3.3	MHz
Clock Duty Cycle	D.C.		40	50	60	%
Delay Time to Data Line Driven[7]	Tdd		18	-	40	ns
Delay Time to Valid Data[7]	Tdv	Max Cload	-	-	100	ns
Delay Time to High Z[7]	Tdz		5	-	16	ns
Hold Time[7]	Thold	Thold, as observed by the input device, will be dependent on Cload	5	-	-	ns

[7] See Figure 1: Timing Diagram.

[8] See Figure 2: Hysteresis Diagram.

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Figure 1: Timing Diagram

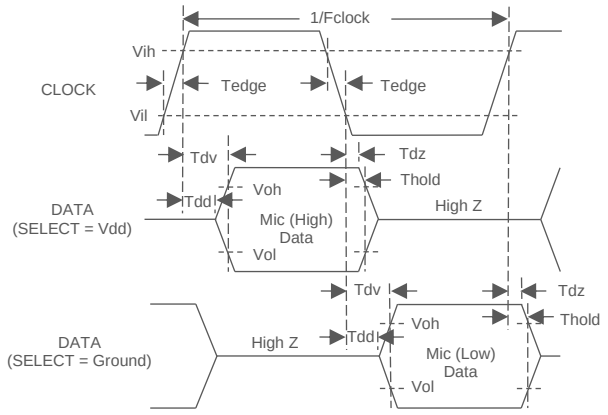


Figure 2: Hysteresis Diagram

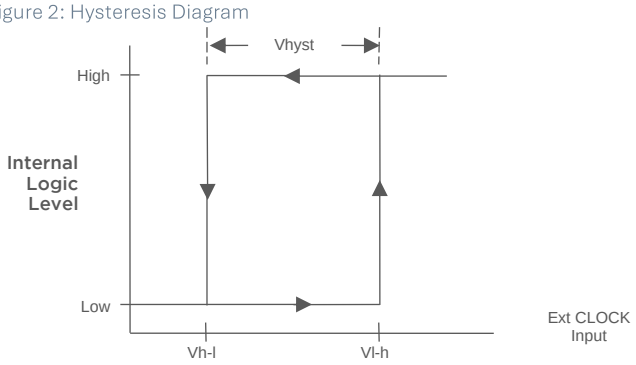


Figure 3: State Diagram

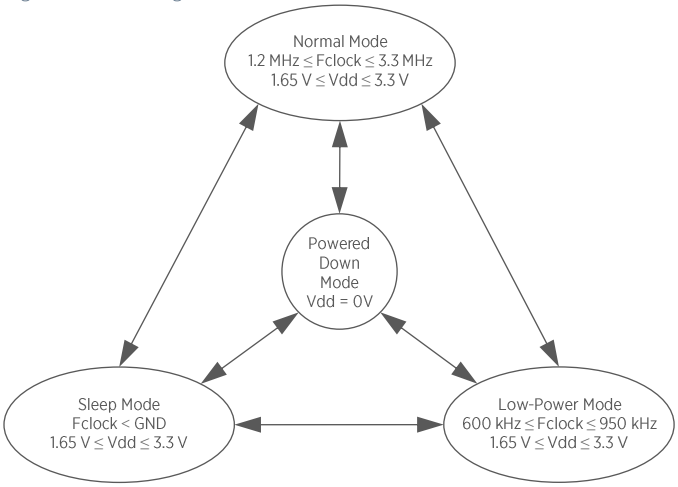


Figure 4: Typical Stereo Application Circuit

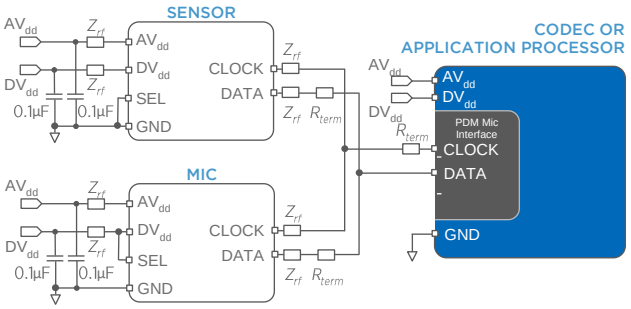
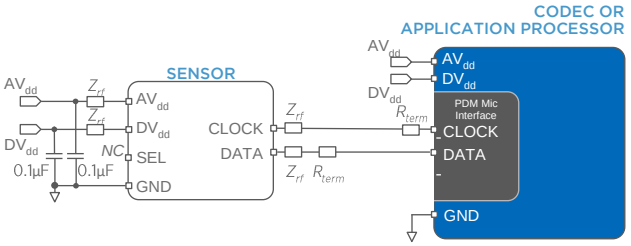


Figure 5: Typical Single-Sensor Application Circuit



NOTES:

All Ground pins must be connected to ground.
If necessary to improve RF performance, optional series components (resistors, ferrites, etc.) should be placed closest to the sensor pads.
Bypass capacitors should be placed near each Vdd pin for best performance.
Capacitors near the sensor should not contain Class 2 dielectrics due to their piezoelectric effect.

Table 7: SELECT Functionality

Sensor	SELECT	Asserts DATA on	Latch DATA on
V2S (High)	Vdd	CLK rising edge	CLK falling edge
V2S (Low)	Ground	CLK falling edge	CLK rising edge

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PERFORMANCE CURVES

Test Conditions: 23 ±2° C, 55 ±20% R.H., Vdd = 1.8 V, Fclock = 2.4 MHz (LPM Fclock = 768 kHz), SELECT grounded, no load, unless otherwise indicated

Figure 6: Typical Acceleration Magnitude

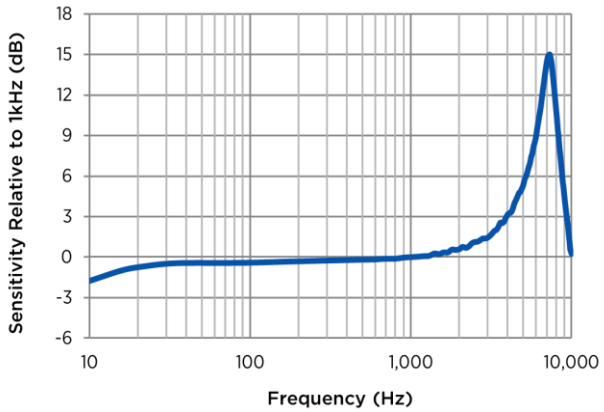

Figure 7: Typical THD vs Acceleration

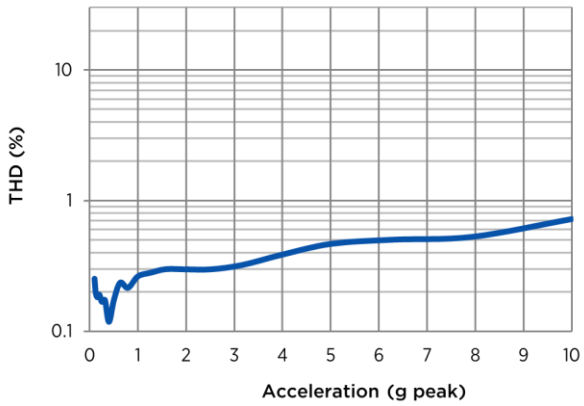

Figure 8: Typical Phase and Group Delay

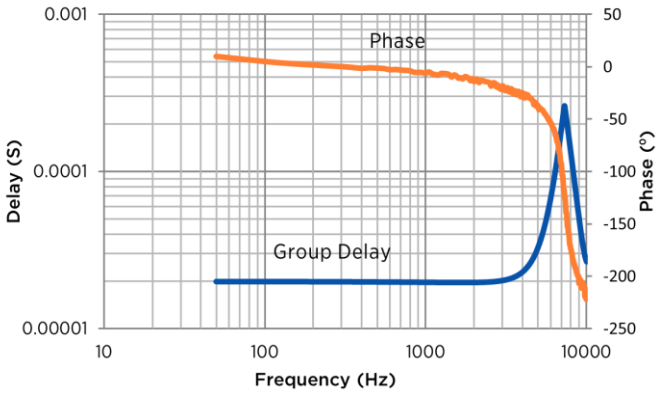

Figure 9: Typical THD vs Frequency (1g peak input)

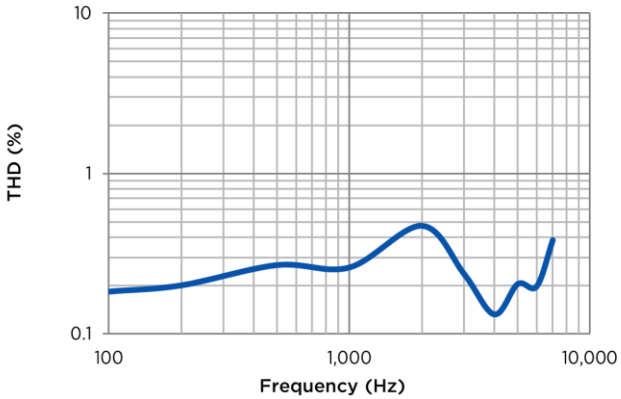

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Figure 10: Typical Idd vs Vdd

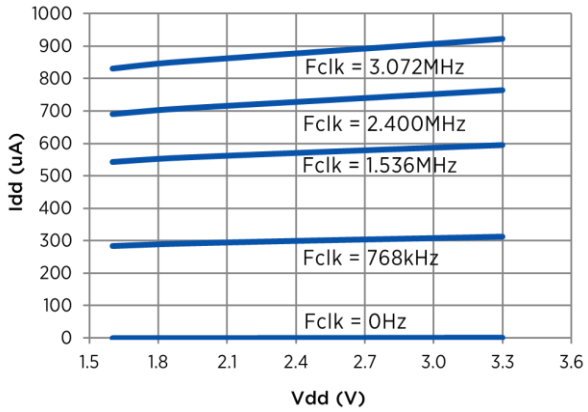


Figure 11: Noise Floor Amplitude Spectral Density

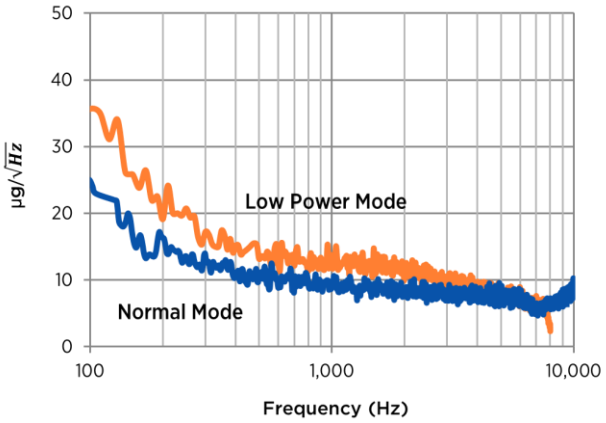
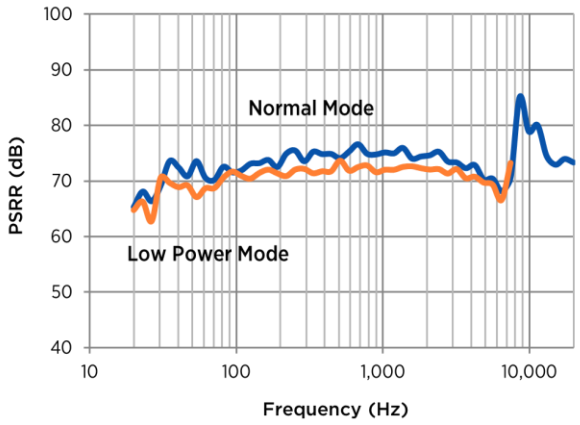


Figure 12: Typical PSRR



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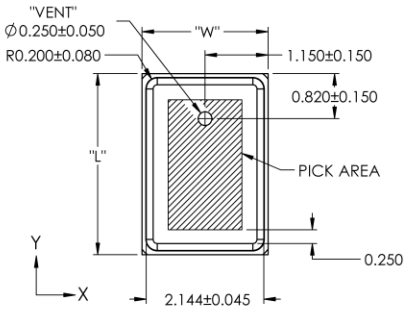
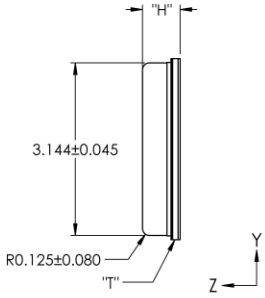
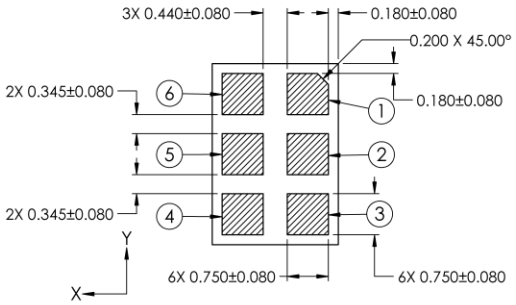
MECHANICAL SPECIFICATIONS



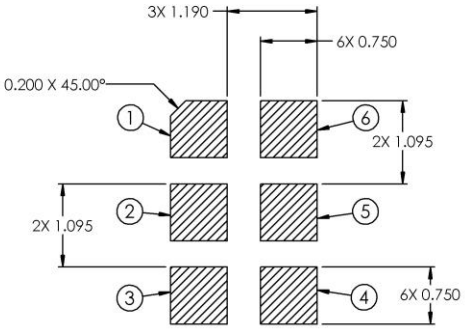




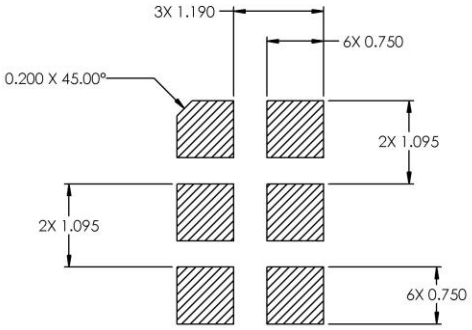
Item	Dimension	Tolerance
Length (L)	3.30	±0.10
Width (W)	2.30	±0.10
Height (H)	0.70	±0.10
PCB Thickness (T)	0.165	±0.05

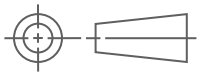
Pin #	Pin Name	Type	Description
1	Vdd	Power	Power Supply
2	CLOCK	Digital I	Clock Input
3, 4	GROUND	Power	Ground
5	SELECT	Digital I	Lo/Hi (L/R) Select
6	DATA	DIGITAL O	PDM Output

Example Land Pattern



Example Solder Stencil Pattern





NOTES:

Pick Area only extends to 0.25 mm of any edge or hole unless otherwise specified. Dimensions are in millimeters unless otherwise specified. Tolerance is ±0.15mm unless otherwise specified. In the acoustic path, «MechanicalsPCBThickness», «MechanicalsGasketDiameter» and «MechanicalsCaseDiameter». Further optimizations based on application should be performed.

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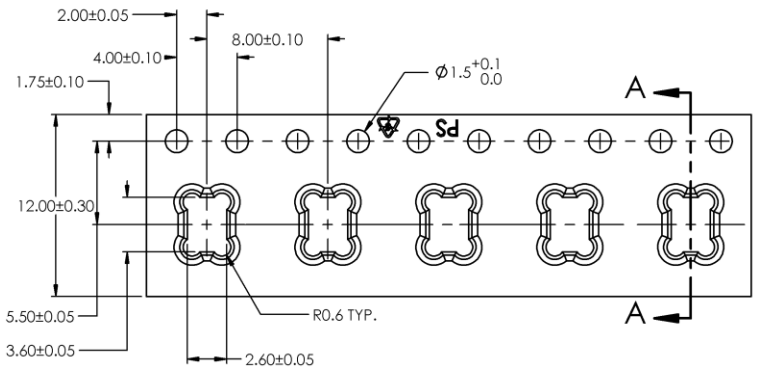
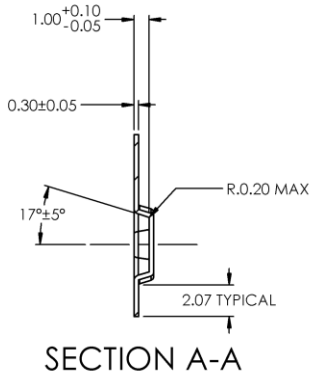
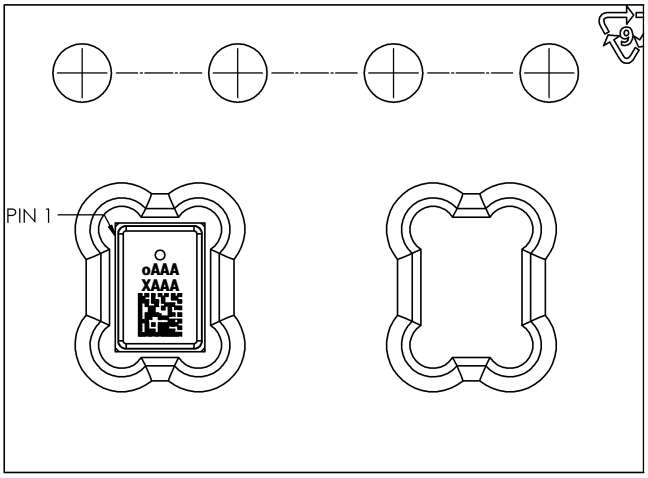
PACKAGING & MARKING DETAIL





Model Number	Suffix	Reel Diameter	Quantity Per Reel
V2S200D-1	-8	13”	5900

Component	Surface Resistance (ohms)
Reel	10^5 - 10^9
Carrier Tape	10^5 - 10^9
Cover Tape	10^4 - 10^{10}



Letter: “o”, orientation mark (pin 1)
AAA = Internal Code
X = Optional Character
AAA = Internal Code
2D barcode "ABCDEFGHJKLMNPQRSTUVWXYZ0123456789":
Unique Job Identification Number for product traceability

NOTES:

Dimensions are in millimeters unless otherwise specified.
Vacuum pickup only in the pick area indicated in Mechanical Specifications.
Tape & reel per EIA-481.
Labels applied directly to reel and external package.
Shelf life: Twelve (12) months when devices are stored in the factory-supplied, unopened ESD moisture sensitive bag under the maximum environmental conditions of 30°C, 70% R.H.

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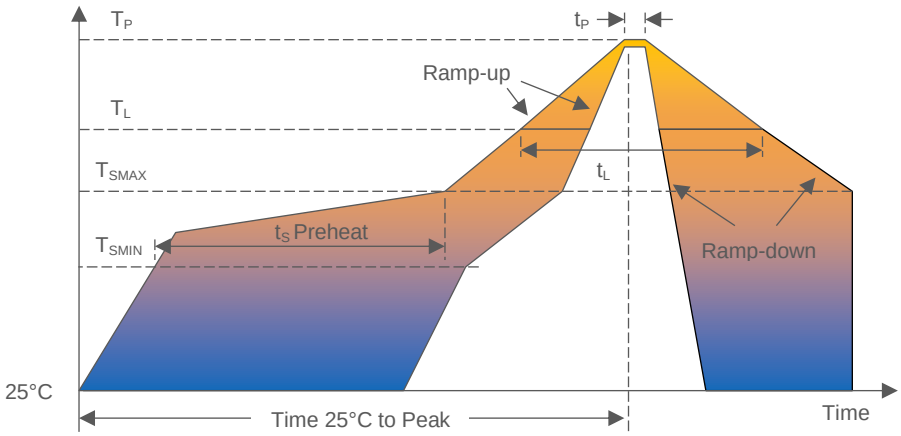
RECOMMENDED REFLOW PROFILE



Profile Feature	Pb-Free
Average Ramp-up rate (T_{SMAX} to T_P)	3°C/second max.
Preheat • Temperature Min (T_{SMIN}) • Temperature Max (T_{SMAX}) • Time (T_{SMIN} to T_{SMAX}) (t_S)	 150°C 200°C 60-180 seconds
Time maintained above: • Temperature (T_L) • Time (t_L)	 217°C 60-150 seconds
Peak Temperature (T_P)	260°C
Time within 5°C of actual Peak Temperature (t_P)	20-40 seconds
Ramp-down rate (T_P to T_{SMAX})	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

NOTES:

Based on IPC/JDEC J-STD-020 Revision C.

All temperatures refer to topside of the package, measured on the package body surface.

The actual reflow profile used should be optimized based on the reflow requirements of all components, board design, solder paste formulation and reflow equipment used. Details of recommended handling and manufacturing processes can be found in AN25 SMT Manufacturing Guidelines for SiSonic™ Microphones.

ADDITIONAL NOTES

(A) Barometric relief hole (vent)
- Hole must be open during reflow.
- No other special treatment is needed on the barometric relief hole during assembly
- If the sensor is exposed to harsh environment, seal the hole with non-porous, low viscosity material (e.g. UV cure, hard plastic overmold)

(B) MSL (moisture sensitivity level) Class 1.

(C) Maximum of 3 reflow cycles is recommended.

(D) In order to minimize device damage:
- Only board wash with deionized water and allow dry time.
- Do not brush board with or without solvents after the reflow process.
- Do not directly expose to vapor phase soldering.
- Do not subject the sensor to strong mechanical agitation.

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MATERIALS STATEMENT

Meets the requirements of the European RoHS directive 2011/65/EC as amended.

Meets the requirements of the industry standard IEC 61249-2-21:2003 for halogenated substances and Syntiant Green Materials Standards Policy section on Halogen-Free.

Product is Beryllium Free according to limits specified on the Syntiant Hazardous Material List (HSL for Products).

Ozone depleting substances are not used in the product or the processes used to make the product, including compounds listed in Annex A, B, and C of the "Montreal Protocol on Substances That Deplete the Ozone Layer.

RELIABILITY SPECIFICATIONS

Test	Description
Thermal Shock	100 cycles of air-to-air thermal shock from -40C to +125C with 15 minute Soaks (IEC 68-2-14)
High Temperature	+105°C environment for 1,000 hours (JESD22-A103)
Low Temperature	-40°C environment for 1,000 hours (JESD22-A119)
ESD-HBM	3 discharges at ±2kV direct contact to I/O pins (ANSI/ESDA/JEDEC JS-001-2014)
ESD-HMM	10 discharges at ±8kV direct contact to lid when unit is grounded (AMSI/ESD SP5.6-2009)
ESD-CDM	3 discharges at ±500V (ANSI/ESDA/JEDEC JS-002-2014)
Reflow	5 reflow cycles with peak temperature of +260°C (JEDEC 22-A113F)
Mechanical Shock	3 pulses of 20,000g in each of the X, Y, Z directions (IEC 68-2-27 Test Ea)
Waterproof	1 meter water submersion for 30 minutes (IPX7)

NOTES:

Sensors meet all performance and electrical specifications before and after reliability testing, except sensitivity which can deviate up to 3dB.

After 3 reflow cycles, the sensitivity of the sensors shall not deviate more than 1 dB from its initial value.

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SPECIFICATION REVISIONS

Revision	Specification Changes	Date
1	Initial Release	2/20/2024
2	IPX7, Maximum G range, remove Ultrasonic welding comment	3/5/2024
3	G range update	5/15/2024
4	Board wash comment Max force exerted on sensor comment Vacuum repacking comment removed Applications added Height tolerance	6/13/2024
5	Updated Mechanical drawings, moved max force exerted on sensor comment	7/19/2024
6	Updated carrier tape drawing	7/23/2024
7	Replaced CAD render with photo	7/27/2024
8	Corrected bandwidth spec	7/31/2024
9	Added IPX7 rating in product features	9/26/2024
10	Clarified stimulus conditions for Sensitivity, SNR, and THD measurements	10/1/2024
11	Updated PSRR spec	10/9/2024
12	Updated PSRR plot, further clarified g peak in specs	11/5/2024
13	Format Update	12/2/2024

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